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Question Paper Code : 51201

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Third Semester

Electronics and Communication Engineering

EC 1201 — DIGITAL ELECTRONICS

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Prove the Boolean theorems : $x + x = x, x.x = x$.
2. What are don't care minterms? State the use of don't care minterms.
3. What do you mean by weighted code? Give an example.
4. Draw the symbol and Truth Table for J-K filp-flop.
5. Draw the logic diagram and give the truth table of half subtractor.
6. State the principle of parity checker.
7. Draw the logic diagram of D flipflop using NAND gates.
8. How does JK filip flop differ from an S–R flip flop in its basic operation?
9. Enumerate the types of ROMs.
10. Compare PAL and PLA devices.

PART B — (5 × 16 = 80 marks)

11. (a) (i) With suitable examples, explain the conversion of standard forms to canonical forms of Boolean expression. (5)

(ii) Implement the given Boolean function $F = xy + x'y' + y'z$ using with NAND and inverter gates. (6)

(iii) Verify, whether or not Exclusive OR operation is commutative and associative. (5)

Or

(b) (i) Show the five variable Karnaugh map and explain the minimization technique. (8)

(ii) Minimize the given Boolean function using Karnaugh map.

$F(A, B, C, D) = \Sigma (0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$. (8)

12. (a) Draw the circuit of TTL NAND gate and explain its operation. Compare the TTL and ECL logic families. (16)

Or

(b) (i) Write a detailed technical note on the interfacing of CMOS and TTL families. (8)

(ii) Explain the switching operation and characteristics of PN junction diode. (8)

13. (a) (i) Design and implement an 8×1 multiplexer using suitable gates. (8)

(ii) Design a 3 bit parity generator and checker circuit. (8)

Or

(b) (i) Design and implement full subtractor using suitable gates. (8)

(ii) Design the logic diagram of magnitude comparator to compare two binary variables A and B accompanied by 3 bits each. (8)

14. (a) (i) Explain the following terms : (8)

(1) Critical race

(2) Hazard

(3) Flow table and flow table reduction

(4) Non critical race.

(ii) Explain the different modes of operation of asynchronous circuits. (8)

Or

(b) (i) Explain the procedure of analyzing asynchronous sequential circuit. (8)

(ii) Explain 4 bit serial in serial out shift register with diagram. (8)

15. (a) Discuss the Programmable Logic Array (PLA). (16)

Or

(b) Explain the following :

(i) Static RAM cell. (8)

(ii) Field Programmable Gate Arrays (FPGA). (8)
